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Guest Editorial

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Chip-Scale Package Reliability-Has It Been Proven?

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Guest Editor

You may have seen summaries from the publication of a NEMI Roadmap earlier this year. You might have wondered, coincidentally, how these diminuative chip scale packages are being used, especially in portable products, and how they can survive the many changes they are subjected to through temperature extremes and mishandling.

You are not alone. Experts from NEMI have similar concerns. While BGAs and CSPs are attractive from an ease-of-assembly perspective, reliability must be improved for BGAs and proven for CSPs. This issue of Chip *Scale Review* on reliability should answer many questions that you have about the assembly reliability of CSPs.

Reliability, irrespective of its definition, is no longer an "after-the-fact" concept; rather, it must be an integral part of development and implementation. This is especially true in the microelectronics field with its uncompromising demands for miniaturization and system integration in a faster, better and lower-cost environment. The rapid development of CSPs and their introduction into the market is a good example of this trend.

Form Factor

CSPs have their own unique form factor not seen in SMT, and many of them may not be able to meet "traditional" reliability test requirements. There has been a paradigm shift in reliability for CSPs and new, specific tests (such as bend and drop) are being adopted to meet consumer portable device requirements. The "shift" is further motivated by several factors, including the following:

- Reduction in life expectancy for consumer electronics
- Rapid changes in electronic technology

For surface mount, solder possesses both electrical and mechanical functions and has been the weakest link in assembly reliability. As a result, damage to solder can readily affect the functional integrity of the microelectronics system. Therefore, understanding the reasons for failure, or defects that cause changes either in mechanical or electrical system characteristics is critical.

Creep and stress relaxation are the main causes of cycling damage. Creep for materials generally occurs at temperatures above half of the absolute melting temperature (T/Tm >0.5). This value is 0.65 at room temperature for eutectic solder (63Sn/37Pb). Thermal damage to solder joints is most often caused by a global CTE (coefficient of thermal expansion) mismatch between the package and board which induces stress. The package and board can also have temperature gradients through the thickness, and at surface areas.

Local CTE mismatch between solder attachment to the component and the PWB.

CTE Mismatch

Reducing the CTE mismatch of component and PWB reduces cycling damage. For leaded surface-mount packages, the CTE mismatch on solder joints is relieved by employing a compliant lead. Rigidity of BGA balls was one of the reliability concerns at the start of their implementation. Experimental test results showed that BGA assembly failed either between ball and package or between ball and PWB (solder joint).

"The most common damage to solder joints is that induced by thermal cycling."

For grid CSPs, the interface between package and solder balls is also a potential failure site. These failure mechanisms indicate that package/solder-joint shear strength is one of the key parameters defining package susceptibility for both thermal and mechanical reliability.

Shear strengths for BGAs and CSPs were measured and compared. For BGAs, package ball shear values ranged from about 1,000 to 1,500 g for plastic and ceramic BGAs. These values represent the 50 percentile shear forces determined from a large number of ball shear tests. Shear forces among CSPs ranged from 170 to about 400 g. Values for wafer packages with low I/O (eight leads) was very low, about 20 g/lead. Shear force depends on many variables, including pad size, metallurgy and configuration attachment, as well as the chemistry of solder.

Deformation

Shear tests will indicate the likelihood of deformation and are especially critical for extreme mechanical conditions. Low values of shear force clearly indicate potential reliability concerns with CSPs. A few CSPs however, have been shown to survive the short duration shock and vibration conditions.

Dynamic behavior is critical for applications of portable products where there is a potential for human mishandling, such as accidental dropping. Dropping tests were performed for the U1traCSP™ (P. Elenius, Pan Pacific 99).

Assemblies were dropped from a height of 1600 mm, achieving a mechanical shock of 8200 G over a period of 0.12 msec. No failure was observed during mechanical shock. Additionally, no failure was observed when the drop height was increased to 2000 mm with a mechanical shock of 12,500 G over a period of 0.11 msec.

Intel has reported mechanical shock test results for the μBGA" package (R. Bauer, J. Malatesta, SMI 98) using Mil Std 883. Fifteen samples were subjected to 1500 G with 0.5 msec duration in the X, Y, and Z axes. No failure was observed after five shock pulses. The testing also showed no failures due to four cycles of vibration in 20-2000 HZ with a 20 G maximum load.

For thermal cycling environments, several inherent features of CSPs strengthen their reliability. These features include reduction in package size (and therefore die size and package thickness). These factors will improve CSP reliability. For high-reliability applications, especially packages with high I/Os, such improvements might not be sufficient, and other innovative technology developments may be required to decrease the local and global CTE mismatch.

New Approaches

Innovative approaches have been developed aimed at absorbing the CTE mismatch between the die and board within the package, or externally through strain absorbing mechanisms, thereby reducing stresses on the solder interconnects.

"Shear tests will indicate the likelihood of deformation and are especially critical for extreme mechanical conditions."

These approaches, however, may introduce their own unique damage mechanisms, since the weakest link now has been transferred from solder to other areas of the attachment system. One new approach uses compliant tape-automated-bonded leads and elastomeric materials between die and substrate to reduce the package CTE mismatch.

Since the TAB leads absorb the majority of stress, this becomes the weakest link and a possible failure site. While this method has been widely shown to be effective for low I/O CSPs, it has yet to be proven for higher I/O CSPs.

The other new approach, called "Floating Pad Design," offers the potential for absorbing the global CTE mismatch. Theoretically, therefore, it can handle a large I/O package. Test results by manufacturers are promising, but they have yet to be verified by others. It is not known yet if such "solder ball floating" will weaken the mechanical strength.

Of course one possible (although undesirable) solution to overcoming the reliability issues is the use of underfill. Underfill application is a common technique which has been widely used for direct attachment of chip-on-board or when package leads are not robust. If everything else fails to improve reliability, underfill might be the ultimate option. Sony employed this method when the company introduced its passportsize camera in early 1997. For other CSPs and environmental conditions, the effectiveness of underfilling still has to be proven.

Do we need to go that far? That's a question that only time, and more experience in the lab and in the field, can answer.

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